DATA SHEET

SA57255-XX

CMOS switching regulator
(PWM controlled)

Product data
Supersedes data of 2001 Aug 01

2003 Nov 11

Philips
Semiconductors

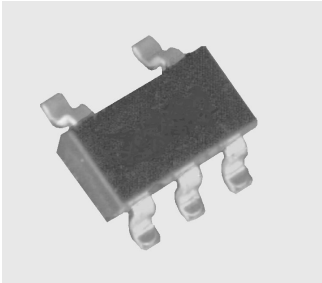
PHILIPS

CMOS switching regulator (PWM controlled) SA57255-XX

GENERAL DESCRIPTION

The SA57255-XX is a highly integrated DC/DC converter circuit. Efficient, compact power conversion is achieved with a pulse width modulation (PWM) controlled switching regulator circuit designed using CMOS processing. Low ripple and high efficiency of typically 83% are achieved through PWM control. The regulator has a high precision output with ±2.4% accuracy. Few external components are required.

The SA57255-XX has a built-in, soft-start circuit to reduce current inrush and voltage overshoot during start up. The PWM control circuit is designed to drive an external low resistance NPN bipolar junction transistor (BJT). The DRIVE output provides typically 7 mA at 100 kHz typical switching frequency to drive the BJT.



FEATURES

- Operates from 0.7 to 9 V_{DC}
- Ultra low operating supply current—typically 17 µA
- Uses external power BJT
- High efficiency—typically 83%
- High precision output—typically ±2.4%
- Operating temperature range of –40 to +85 °C
- Available output voltages: 2.0, 2.5, 2.8, 3.0, 3.3, 3.6, 5.0 V_{DC}
- Available in a 5-lead small outline surface mount package (SOP003)

APPLICATIONS

- Mobile and portable phones
- Instrumentation and industrial products
- Other portable, battery-operated equipment

SIMPLIFIED SYSTEM DIAGRAM

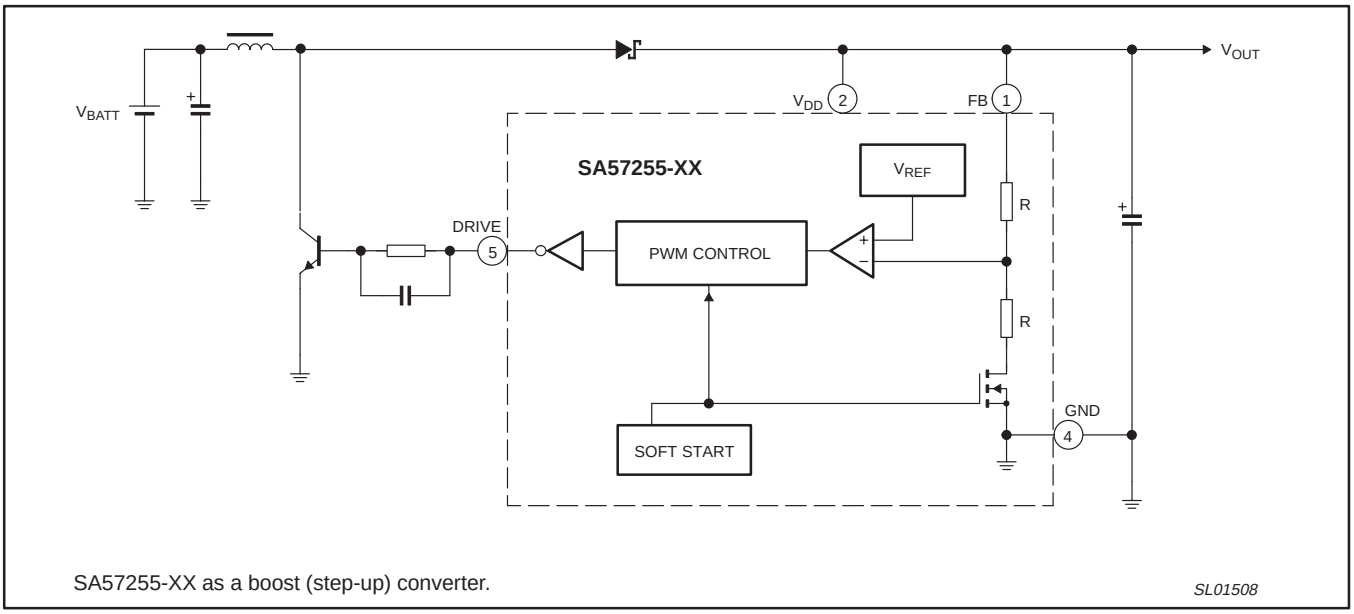


Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
SA57255-**XX**GW	SOT23-5, SOT25, SO5	Plastic small outline package; 5 leads; body width 1.6 mm	SOP003	–40 to +85 °C

NOTE:
The device has seven voltage output options, indicated by the **XX** on the Type Number.

XX	VOLTAGE (Typical)
20	2.0 V
25	2.5 V
28	2.8 V
30	3.0 V
33	3.3 V
36	3.6 V
50	5.0 V

Part number marking

Each device is marked with a four letter code. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code.

Part number	Marking
SA57255-20GW	A E T x
SA57255-25GW	A E U x
SA57255-28GW	A E V x
SA57255-30GW	A E W x
SA57255-33GW	A E X x
SA57255-36GW	A E Y x
SA57255-50GW	A E Z x

PIN CONFIGURATION

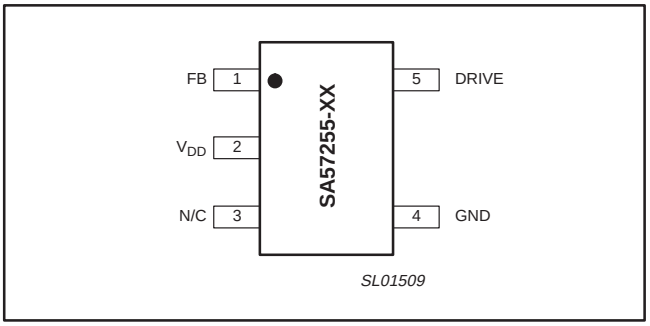


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	FB	Feedback from the output voltage to the PWM control.
2	V_{DD}	Voltage input to regulator.
3	N/C	No connection.
4	GND	Ground.
5	DRIVE	Output for external power transistor.

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{FB}	FB pin voltage	–0.3	11	V
$V_{DD(max)}$	Power supply voltage	–0.3	11	V
V_{DRIVE}	DRIVE pin voltage	–0.3	11	V
I_{DRIVE}	DRIVE pin current	–	300	mA
T_{oper}	Operating temperature	–40	+85	°C
T_{stg}	Storage temperature	–40	+125	°C
P_D	Power dissipation	–	150	mW

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	Part #	MIN.	TYP.	MAX.	UNIT
V_{IN}	input voltage		–	–	–	9.0	V
V_{ST1}	operating start voltage	I_{OUT} = 1.0 mA	–	–	–	0.9	V
V_{ST2}	oscillator start voltage		–	0.7	–	0.8	V
V_{HLD}	operation hold voltage	I_{OUT} = 1.0 mA	–	0.7	–	–	V
I_{SS1}	consumption current 1	V_{OUT} = output voltage × 0.95	-20	–	14.5	24.1	µA
			-25	–	17.8	29.7	µA
			-28	–	20.0	33.3	µA
			-30	–	21.4	35.7	µA
			-33	–	23.7	39.5	µA
			-36	–	28.8	48.0	µA
			-50	–	54.0	89.9	µA
I_{SS2}	consumption current 2	V_{OUT} = output voltage + 0.5 V	-20	–	3.8	7.6	µA
			-25	–	3.9	7.7	µA
			-28	–	3.9	7.8	µA
			-30	–	3.9	7.8	µA
			-33	–	4.0	7.9	µA
			-36	–	4.0	7.9	µA
			-50	–	4.2	8.3	µA
I_{DRIVEH}	DRIVE pin output current (HIGH)	$V_{DRIVE} = V_{OUT} – 0.4$ V	-20	–	–1.9	–2.9	mA
			-25	–	–2.7	–4.0	mA
			-28	–	–2.7	–4.0	mA
			-30	–	–3.5	–5.3	mA
			-33	–	–3.5	–5.3	mA
			-36	–	–3.5	–5.3	mA
			-50	–	–5.3	–8.0	mA
I_{DRIVEL}	DRIVE pin output current (LOW)	V_{DRIVE} = 0.4 V	-20	–	3.8	5.7	mA
			-25	–	5.3	8.0	mA
			-28	–	5.3	8.0	mA
			-30	–	7.0	10.5	mA
			-33	–	7.0	10.5	mA
			-36	–	7.0	10.5	mA
			-50	–	10.7	16	mA
ΔV_{OUT2}	load ripple voltage	I_{OUT} = 10 mA ≈ I_{OUT} (following) × 1.25	–	–	30	60	mV
$\Delta V_{OUT}/\Delta T_{amb}$	output voltage temperature coefficient	–40 °C ≤ T_{amb} ≤ +85 °C	–	–	±50	–	ppm/°C
f_{OSC}	oscillator frequency	V_{OUT} = output voltage × 0.95	–	85	100	115	kHz
MaxDuty	maximum duty ratio	V_{OUT} = output voltage × 0.95	–	80	83	86	%
t_{SS}	soft start time	I_{OUT} = 1.0 mA	–	3.0	6.0	12	ms
E_{FFI}	efficiency		-20	–	76	–	%
			-25	–	80	–	%
			-28	–	80	–	%
			-30	–	84	–	%
			-33	–	84	–	%
			-36	–	84	–	%
			-50	–	88	–	%

TYPICAL PERFORMANCE CURVES

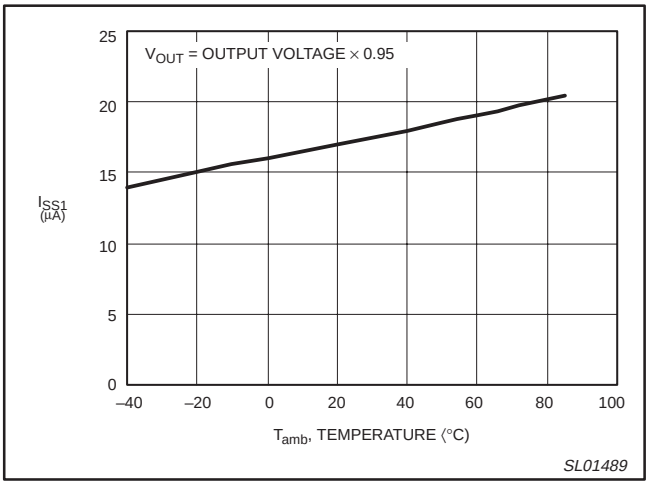


Figure 3. Supply current 1 versus temperature.

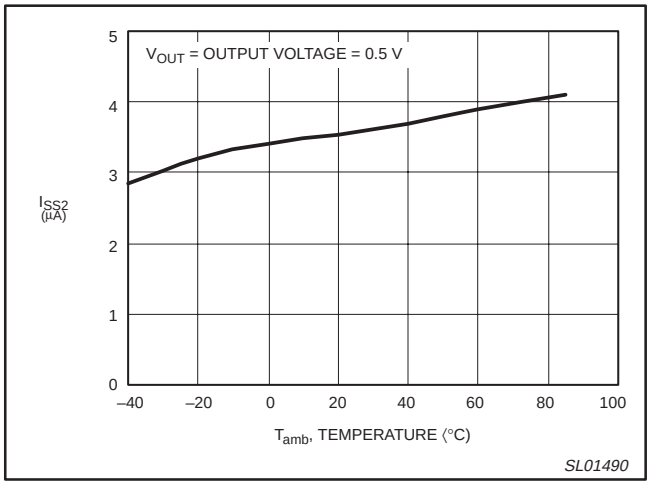


Figure 4. Supply current 2 versus temperature.

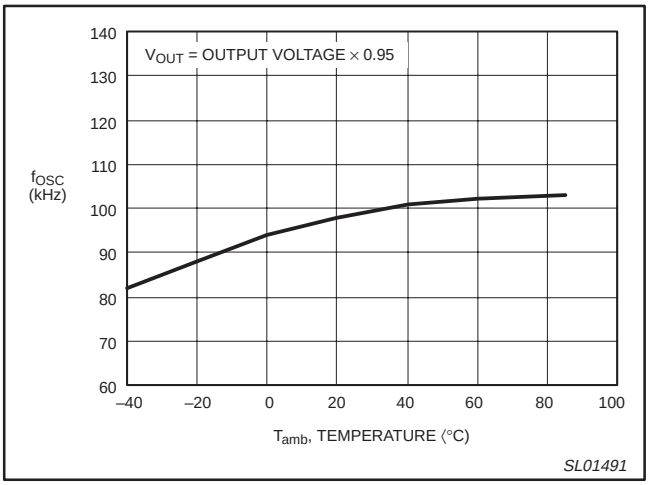


Figure 5. Oscillator frequency versus temperature.

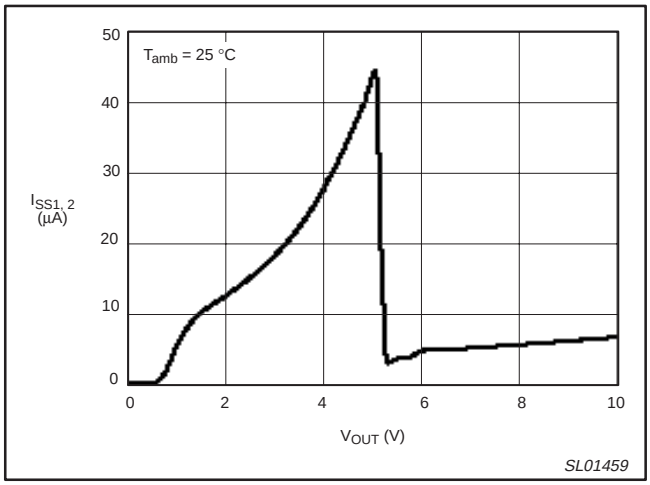


Figure 6. Supply current 1, 2 versus V_{OUT}.

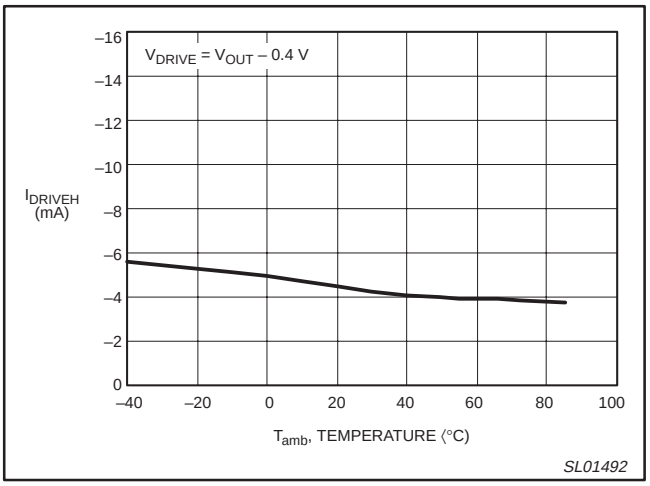


Figure 7. DRIVE pin output current HIGH versus temperature.

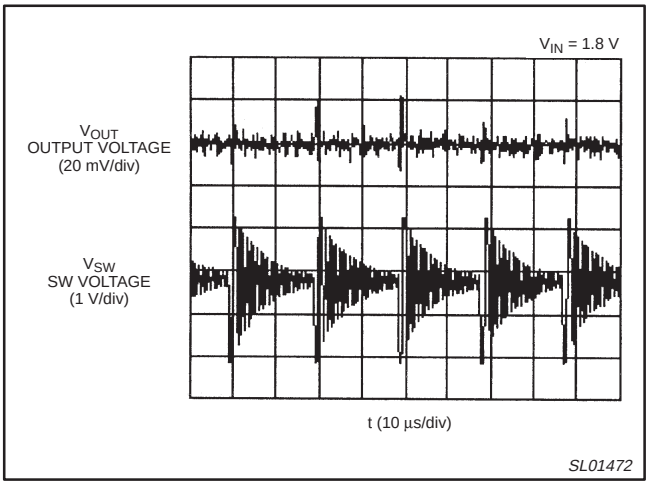


Figure 8. Ripple voltage with light load.

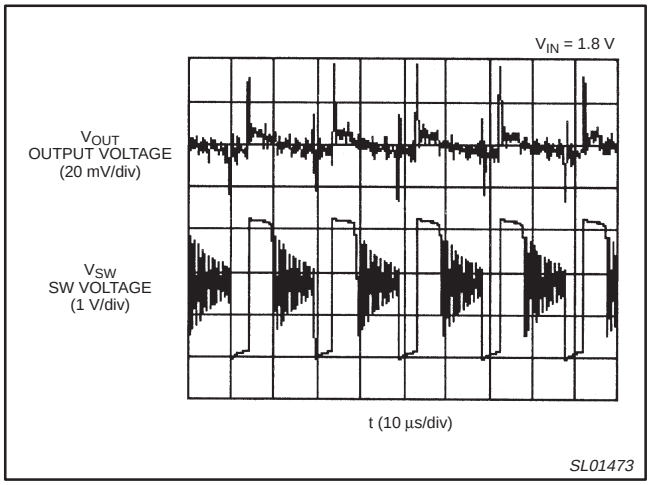


Figure 9. Ripple voltage with medium load.

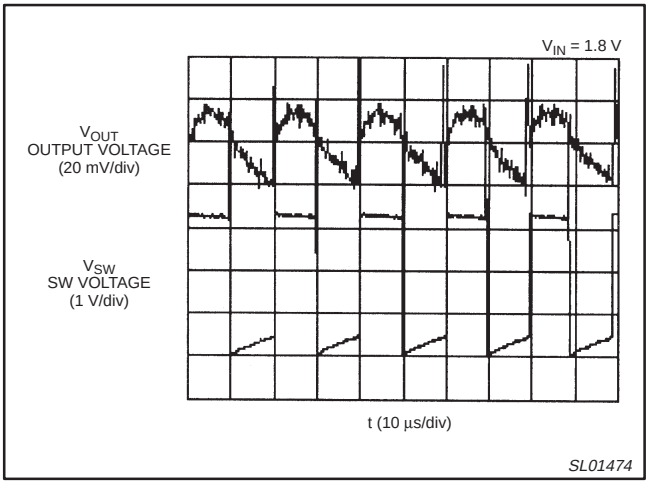


Figure 10. Ripple voltage with heavy load.

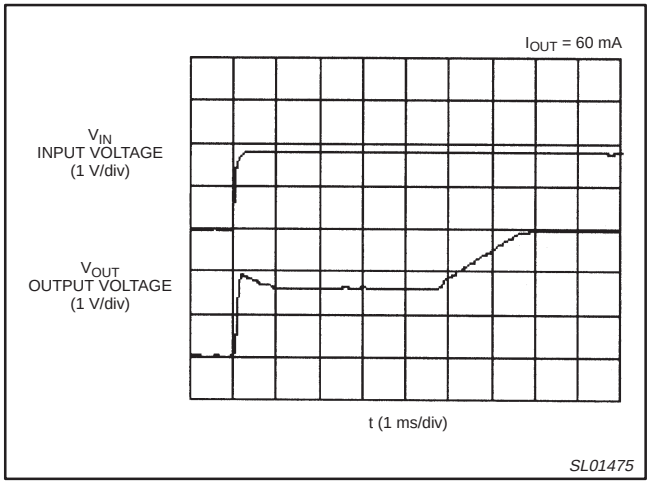


Figure 11. Start-up characteristic V_{IN}: 0 V → 1.8 V.

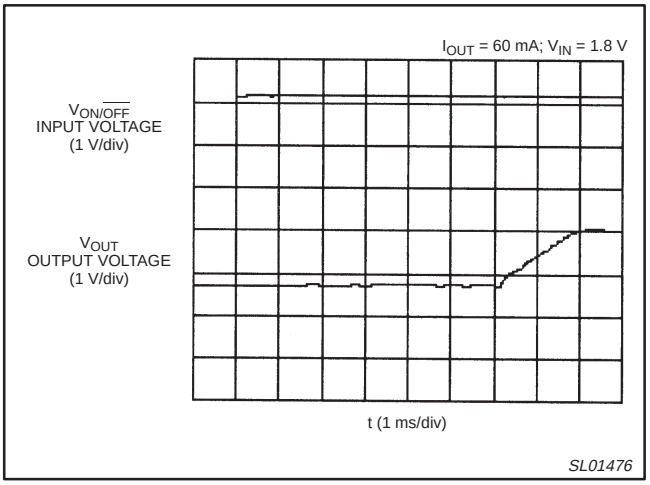


Figure 12. Start-up characteristic $V_{ON/\overline{OFF}}$: 0 V → 3.0 V.

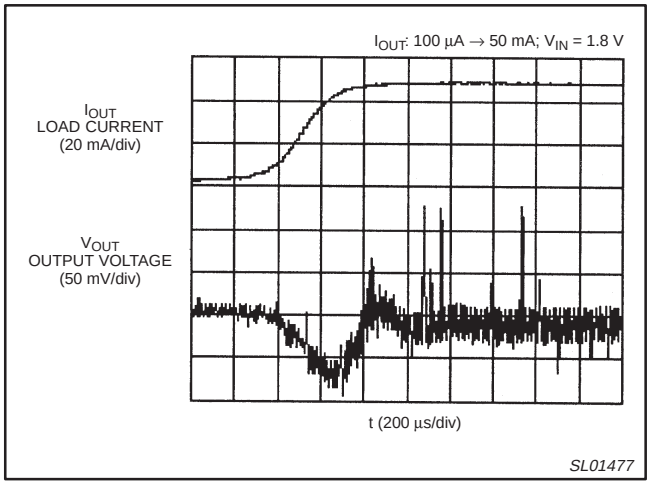


Figure 13. Output load regulation, increasing current.

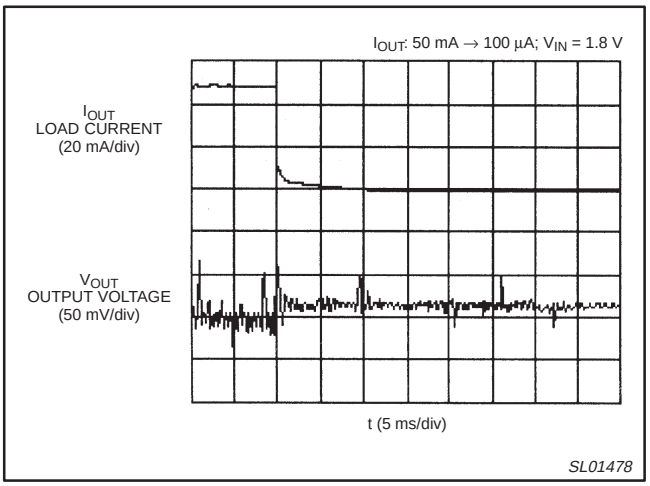


Figure 14. Output load regulation, decreasing current.

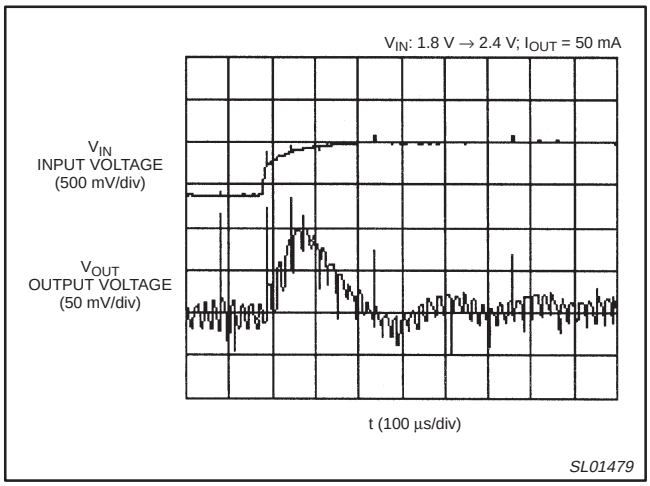


Figure 15. Input line regulation, increasing voltage.

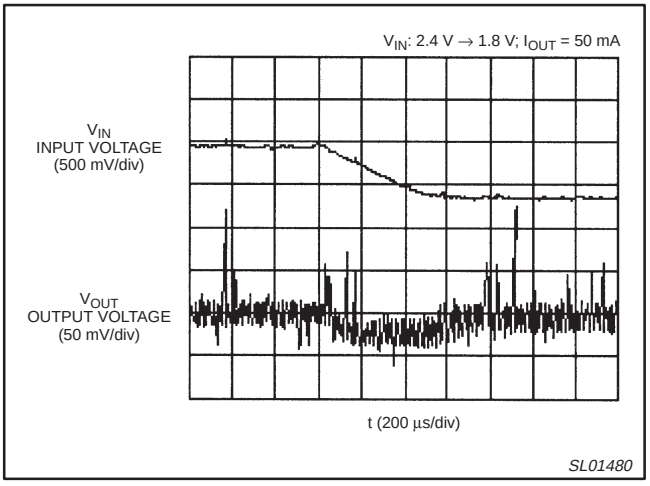


Figure 16. Input line regulation, decreasing voltage.

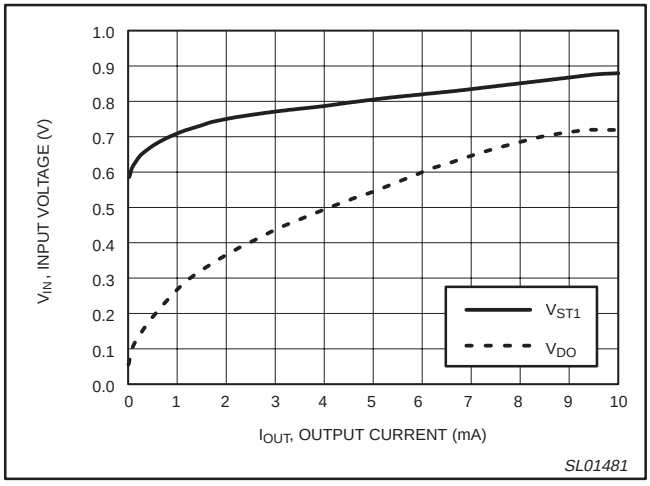


Figure 17. Output current versus starting voltage.

TECHNICAL DISCUSSION

General discussion

The SA57255-XX is a fixed frequency, boost-mode switching power supply controller. Each device is set to provide a fixed output voltage by having a fully compensated internal voltage feedback loop. The SA57255-XX operates at a fixed frequency of 100 kHz and can operate from a single alkaline cell (0.9 V) or up to 9 V.

The SA57255-XX requires an external NPN bipolar transistor to provide the switching power waveform. Its internal block diagram is shown in Figure 18.

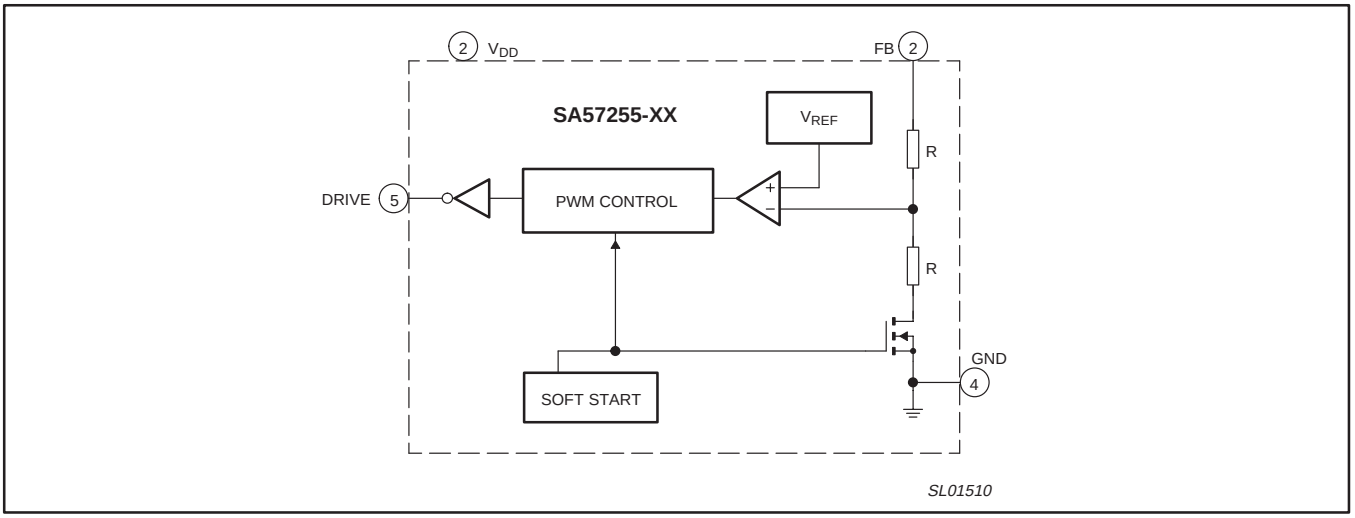


Figure 18. Functional diagram.

APPLICATION INFORMATION

The SA57255-XX can be used for a simple boost (step-up) converter or the less commonly used flyback converter (isolated boost). The major operating restriction of the simple boost converter is that its output voltage **must** always be above the highest expected value of the input voltage. The flyback converter circuit requires more parts, but the output voltage is not restricted by the input voltage.

Boost converter fundamentals

The boost or step-up converter is a non-dielectrically isolated switching power supply topology (arrangement of power parts). That is, the input power source is directly connected to the output load (ground and signals). A typical boost converter, with an optional passive snubber, can be seen in Figure 19.

To understand the boost converter's operation, examine its three periods of operation. These periods are: the power switch on-time (period 1); the inductor discharge period (period 2); and the inductor empty state (period 3). These periods and their associated currents can be seen in Figure 20.

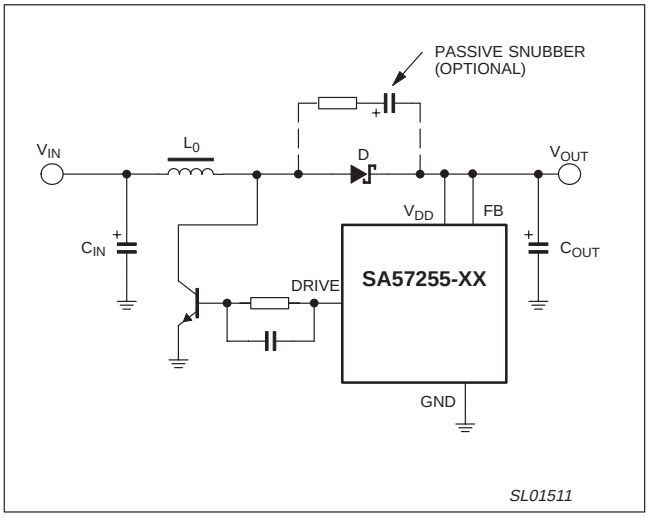


Figure 19. Boost converter.

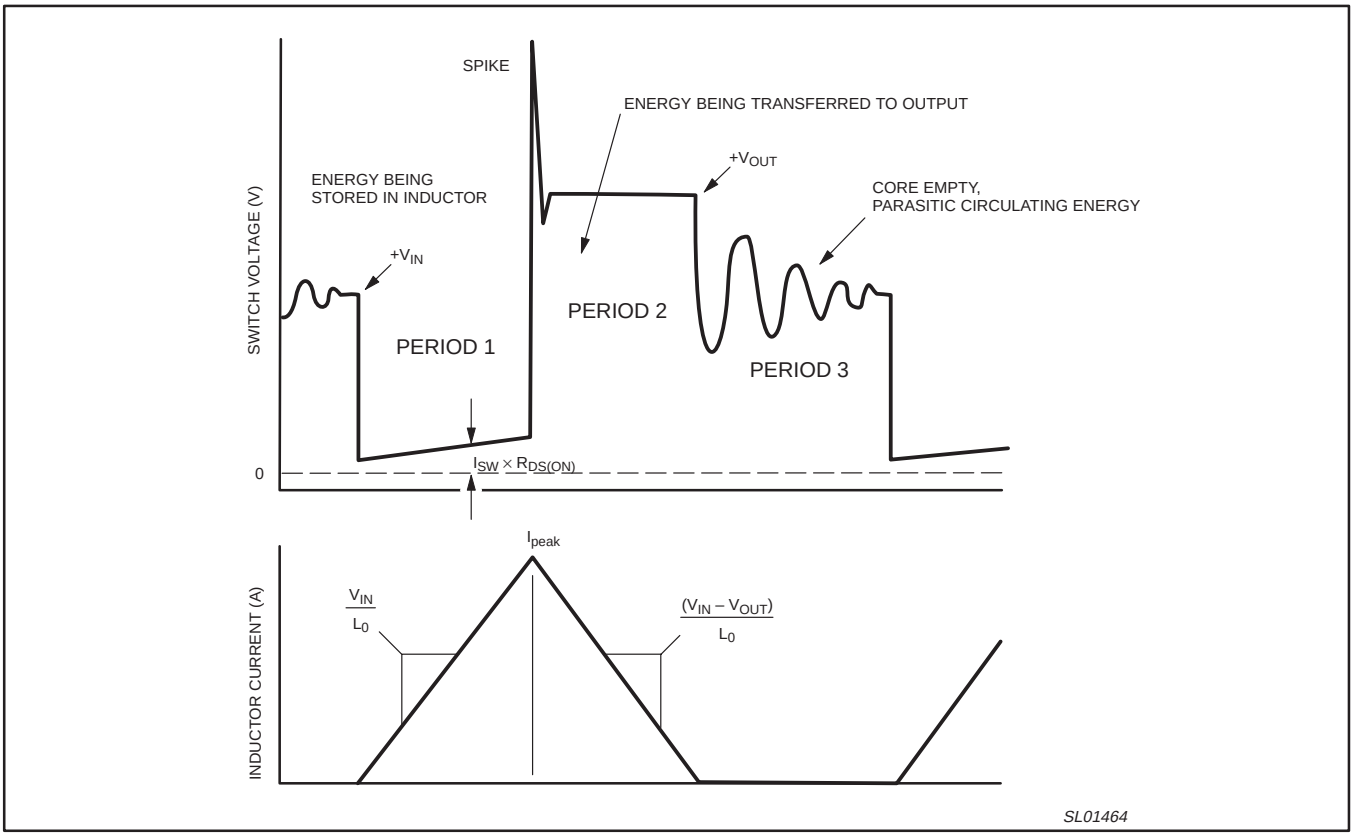


Figure 20. Boost converter waveforms (discontinuous mode).

Period 1: power switch on-time
During this period, a simple circuit loop is formed when the power switch is on. The input voltage source is connected directly across the boost inductor (L_0). A current ramp is exhibited whose slope is described by:

$$IL_{(on)} = \frac{V_{IN}}{L_0} \quad \textbf{Eqn. (1)}$$

Energy is then stored within the core material of the inductor and is described by:

$$E_{sto} = 0.5L_0 \times I_{peak}^2 \quad \textbf{Eqn. (2)}$$

This current ramp continues until the controller turns off the power switch.

Period 2: inductor discharge period
The instant the power switch turns off, the current flowing through the inductor forces the voltage at its output node (switched node) to rise quickly above the input voltage (spike). This voltage is then clamped when it exceeds the device's output voltage and the output rectifier becomes forward biased. The inductor empties its stored energy in the form of a linearly decreasing current ramp whose slope is dictated by:

$$I_{L(off)} \approx \frac{V_{IN} - V_{OUT}}{L_0} \quad \textbf{Eqn. (3)}$$

The stored energy is transferred to the output capacitor. This output current continues until the magnetic core is completely emptied of its stored energy or the power switch turns back on.

Period 3: inductor empty state

DISCONTINUOUS MODE—This period as displayed in Figure 20 occurs in the discontinuous–mode of operation of a boost converter. It is identified by a period of "ringing" following the output period (period 2). The inductor has been completely emptied of its stored energy and the switched node returns to the level of the input voltage. Ringing is seen at this node because a resonant circuit is formed by the inductance of L_0 and any parasitic inductances and capacitances connected to that node. This ringing has very little energy and can easily be eliminated by a small passive snubber.

CONTINUOUS MODE—If the inductor is not completely emptied of its stored energy before the power switch turns on again, the converter is operating in the continuous mode. A small amount of residual flux (energy) remains in the inductor core and the current waveform jumps to an initial value when the power switch is again turned-on. This mode offers some advantages over the discontinuous-mode, because the peak current seen by the power switch is lower. In low voltage applications, the inductor can store more energy with lower peak currents.

The continuous mode waveforms can be seen in Figure 21.

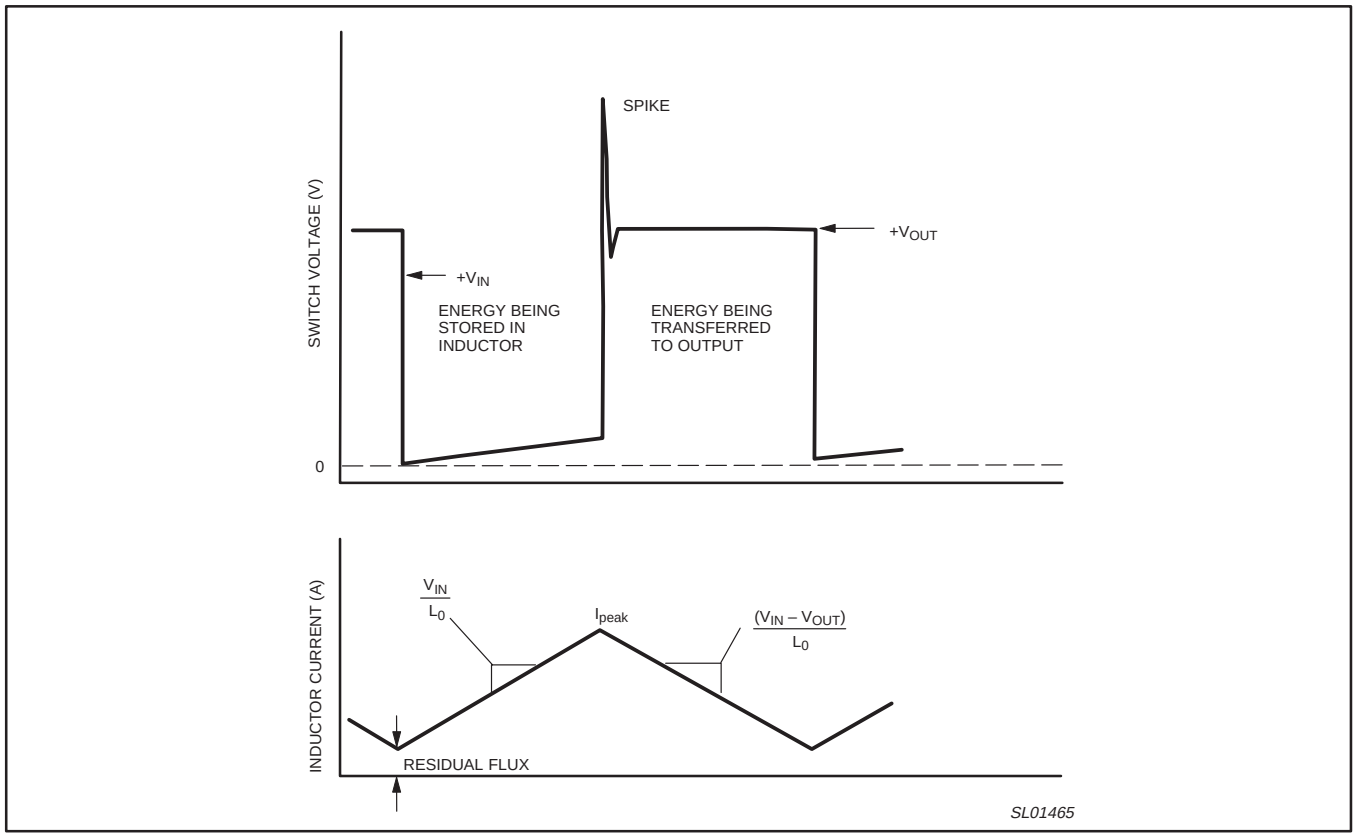


Figure 21. Continuous mode waveforms.

Selecting the external NPN transistor
The SA57255-XX requires an external NPN bipolar transistor to provide the PWM switching waveform to the boost power circuit. The type of bipolar transistor for this power range includes higher current “small signal” transistors or “medium power” transistors.

Minimum transistor parameters are:

Case: minimum $P_{D(max)}$	800 mW (such as SOT223)
$HFE_{(min)}$	100
VCEO	20 V
$IC_{(max)}$	500 mA minimum

A good choice for 0.5 watts and below is the PZT2222A, which exceeds these specifications.

Determining the value of the boost inductor
The precise value of the boost inductor is not critical to the operation of the SA57255-XX. The value of the boost inductor should be calculated to provide continuous-mode operation over most of its operating range. The converter may enter the discontinuous-mode when the output load current falls to less than about 20 percent of the full-load current.

At low input voltages, the time required to store the needed energy lengthens, but the time needed to empty the inductor’s core of its energy shrinks. Conversely, at high input voltages, the time needed to store the energy shrinks while the time needed to empty the core increases. See Equations (1) and (3). At the extremes of these conditions, the converter will fall out of regulation, that is the output voltage will begin to fall, because the time needed for either storing or emptying the stored inductor energy is too short to support the output load current.

Equation (4) determines the nominal value of the inductance.

$$L0 \cong \frac{V_{IN(min)} \times T_{on}}{I_{peak}} \qquad \textbf{Eqn. (4)}$$

Where:
$V_{IN(min)}$ is the lowest expected input operating voltage (V).
T_{on} is about 5 µs or one-half the switching period (s).
I_{peak} is the maximum peak current for the NPN transistor.

This is an estimated inductor value and you can select an inductance value slightly higher or lower with little effect on the converter’s operation. If the design falls out of regulation within the desired operating range, reduce the inductance value, but by no more than 30 percent.

Determining the minimum value of the capacitors
The input and output capacitors experience the current waveforms seen in Figures 20 and 21. The peak currents can be typically between 3 to 6 times the average currents flowing into the input and from the output. This makes the choice of capacitor an issue of how much ripple voltage can be tolerated on the capacitor’s terminals and how much heating the capacitor can tolerate. At the power levels produced by the SA57255-XX heating is not a major issue.

The Equivalent Series Resistance (ESR) of the capacitor, the resistance that appears between its terminals, and the actual capacitance causes heat to be generated within the case whenever there is current entering or exiting the capacitor. ESR also adds to the apparent voltage drop across the capacitor. The heat that is generated can be approximated by Equation (5).

$$P_D(\textit{in watts}) \cong (1.8 I_{av})^2 \ (R_{ESR}) \qquad \textbf{Eqn. (5)}$$

ESR’s effect on the capacitor voltage is given by Equation (6).

$$\Delta V_C \cong I_{peak}(R_{ESR}) \qquad \text{(expressed as } V_{p-p}) \qquad \textbf{Eqn. (6)}$$

A ceramic capacitor would typically be used in this application if the required value is less than 1 – 10 µF, or a tantalum capacitor for required values of 10 µF and above. Lower cost aluminum electrolytic capacitors can be used, but you should confirm that the higher ESRs typically exhibited by these capacitors does not cause a problem.

The minimum value of the output capacitor can be estimated by Equation (7).

$$C_{OUT} > \frac{(I_{OUT(max)}) \ (T_{off})}{V_{ripple(p-p)}} \qquad \textbf{Eqn. (7)}$$

Where:
I_{OUT} is the average value of the output load current (A).
T_{off} is the nominal off–time of the power switch (sec) [≅10 µs].
V_{ripple} is the desired amount of ripple voltage (V_{p-p}).

Finding the value of the input capacitor is done by Equation (8).

$$C_{IN} > \frac{(I_{peak}) \ (T_{on})}{V_{drop}} \qquad \textbf{Eqn. (8)}$$

Where:
I_{peak} is the expected maximum peak current of the switch (A).
T_{on} is the on-time of the switch (sec) [≅10 µs].
V_{drop} is the desired amount of voltage drop across the capacitor (V_{p-p}).

These calculations should produce a good estimate of the needed values of the input and output capacitors to yield the desired ripple voltages.

Selecting the output rectifier
The output rectifier (D) is critical to the efficiency and low-noise operation of the boost converter. The majority of the loss within the supply will be caused by the output rectifier. Three parameters are important in the rectifier’s operation within a boost-mode supply. These are defined below.

Forward voltage drop (V_f)—This is the voltage across the rectifier when a forward current is flowing through the rectifier. A P-N ultra-fast diode exhibits a 0.7 – 1.4 volt drop, and this drop is relatively fixed over the range of forward currents. A Schottky diode exhibits a 0.3 – 0.6 volt drop and appears more resistive during the forward conduction periods. That is, its forward voltage drop increases with increasing currents. You can gain an advantage by purposely over-rating the current rating of a Schottky rectifier.

Reverse recovery time (T_{rr})—This is an issue when the boost supply is operating in the continuous-mode. T_{rr} is the amount of time required for the rectifier to assume an open circuit when a forward current is flowing and a reverse voltage is then placed across its terminals. P-N ultra-fast rectifiers typically have a 25–40 ns reverse recovery time. Schottky rectifiers have a very short or no reverse recovery time.

Forward recovery time (T_{fr})—This is the amount of time before a rectifier begins conducting forward current after a forward voltage is placed across its terminals. This parameter is not always well specified by the rectifier manufacturers. It causes a spike to appear when the power switch turns off. This particular point in its operation causes the most radiated noise. Several rectifiers may have to be evaluated for the prototype. After the final output rectifier selection is made, if the spike is still causing a problem a small passive snubber can be placed across the rectifier.

For this boost application, the best choice of output rectifier is a low forward drop, 0.5 – 1 ampere, 20 volt Schottky rectifier such as the Philips part number BAT120A.

Flyback converter

The SA57255-XX can also be used to create a flyback converter, also known as an isolated boost converter. The advantage of a flyback converter is that the input voltage can go higher or lower than the output voltage without affecting the operation of the converter. The only restrictions are the breakdown voltage of the NPN transistor and the feedback (V_{FB}) pins.

One transformer can accommodate a variety of output voltages in different applications, because the circuit will change the on and off–times to provide the desired output voltage.

The output voltage of the flyback can be changed by using a SA57255-XX with the desired output voltage, with no other changes to the circuit.

Selecting the components

It is best to operate the transformer in the continuous-mode where the highest expected peak primary current is below the maximum current rating of the NPN transistor.

Begin with a peak current equal to or less than the maximum current rating of the NPN transistor. A reasonable value of the primary inductance can be found in Equation (9).

$$L_{pri} < 5V_{IN(min)} \times \frac{T_{on}}{I_{peak}} \qquad \textbf{Eqn. (9)}$$

Where:

I_{peak} is the current rating of the NPN transistor.
T_{on} is the maximum expected on-time of the switch (≈10 μs).
$V_{IN(min)}$ is the lowest expected input voltage (V).

Then select an off-the-shelf transformer such as the Coiltronics CTX100–1P, a 1:1 turns ratio transformer that has a primary inductance of 100 μH. It does not reach saturation until the primary current reaches 440 mA, which is above the expected peak current of the flyback converter. The 1:1 turns ratio should work for output voltages from 0.8 to 2 times the highest input voltage, and produce the output voltage set by the SA57255-XX. The only other restriction is that the input voltage plus the output voltage must be less than the breakdown voltage of the NPN transistor.

Use Equation (8) to determine the minimum value for the input capacitor. A 0.1 V drop is desired across this capacitor.

$$C_{IN} > \frac{(0.3A)\ (10\mu s)}{0.1V} = 30\mu F$$

A 47 μF at 6 V tantalum capacitor would be suitable.

For the design example, the output voltage will be +3.3 V with a maximum output current of 50 mA. The input voltage can vary between +1.8 V and 4.0 V. The design can be seen in Figure 22, and the expected waveforms can be seen in Figure 23.

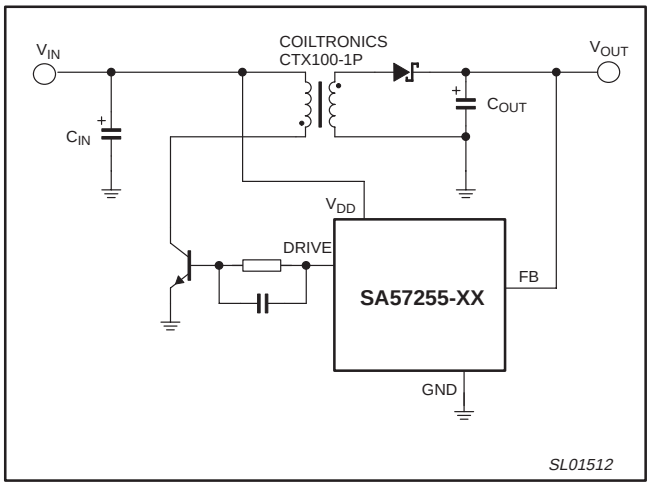


Figure 22. Flyback converter circuit.

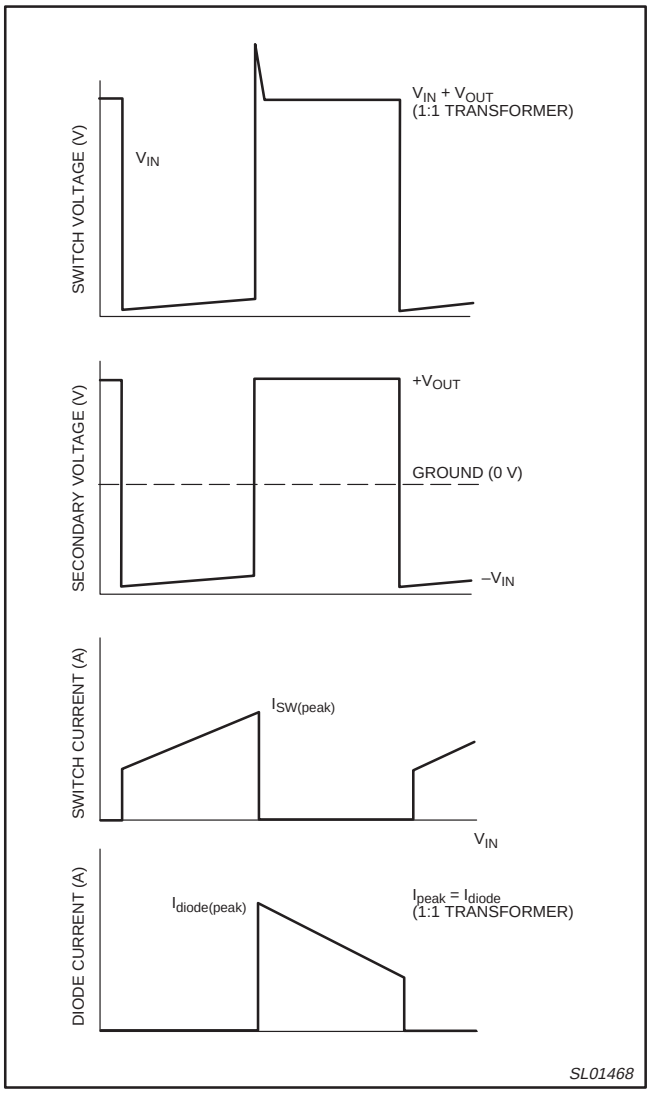


Figure 23. Flyback converter waveforms.

Designing a passive snubber

If the switching power supply is generating too much radio frequency interference (RFI) a **passive snubber** can be added. A passive snubber is a series resistor and capacitor placed across any component that exhibits a resonant “ringing”. This series R-L-C loop creates a lossy or damped tank circuit that dissipates the ringing energy. The design is critical, because it introduces another loss within the converter.

Designing a snubber is an empirical process, mainly because it involves undefined parasitic capacitances and inductances contributed by the PCB layout, leakage inductance, and device capacitances. The snubber should be placed across the major source of the spike or ringing which is the output rectifier.

The usual design process is:

1. Measure the period of the undesired ringing (T_0).
2. Place a very small ceramic capacitor (about 10 pF) across the output rectifier or primary winding.
3. Re-measure the period of the undesired ringing. The new period should be about 3 times that of T_0. If it is less than this, place a slightly larger value of capacitor across the output rectifier or primary winding.
4. Once the desired increase in the ringing period is achieved with a capacitance (C_0), place a resistor in series with the capacitor whose value is approximately:

$$R_{snubber} \cong \frac{T_0}{2\pi C_0} \qquad \textbf{Eqn. (10)}$$

This should produce a snubber that does not load the circuit and introduces a very small loss.

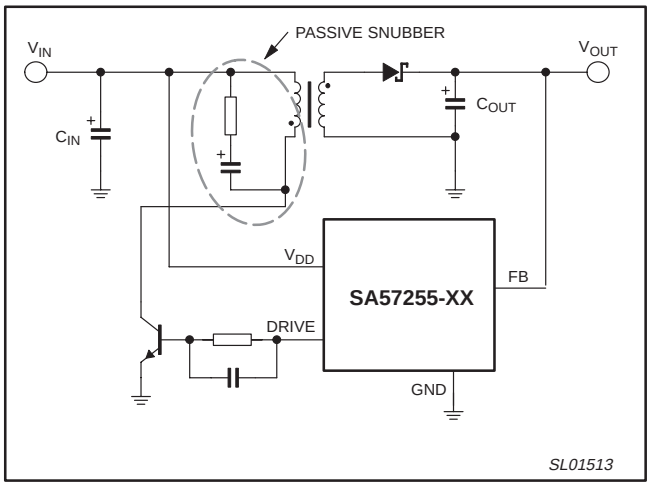


Figure 24. Flyback converter with passive snubber.

Laying out the printed circuit board

The design of the printed circuit board (PCB) is critical to the proper operation of all switching power supplies. Its design affects the supply stability, radio frequency interference behavior and the reliability of the converter.

Never use the **autoroute** feature of any PCB design program because this will always produce traces that are too long and too thin.

The input and output capacitors are the only source or sink of the high frequency currents found in a switching power supply. All connections to the switching power supply from the outside circuits should be made to the input or output capacitor terminals (+ and –). Internally, the layout should adhere to a “one-point” grounding system, as shown in Figure 25.

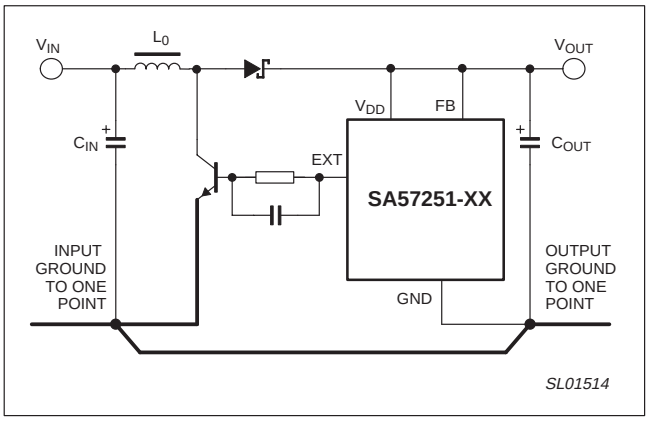


Figure 25. Grounding trace for converter.

The traces between the input and output capacitors and the inductor, power switch and rectifier(s) should be as short and wide as possible. This reduces the series resistance and inductance that can be introduced by traces.

The guidelines for a PCB layout can be summarized as:

- The traces between the input and output capacitor to the inductor, power switch and the rectifier should be made as short and as wide as possible.
- Strictly adhere to the one-point wiring practices shown in Figure 25.
- On a 2-sided board, do not run sensitive signals traces under the AC voltage node.
- The IC (control) ground is terminated at the output capacitor’s negative terminal.

Designing the PCB for effective heat dissipation

The maximum junction temperature is +125 °C which should not be exceeded under any operating conditions. Designing a PCB that includes a heatsink system under the device is the key to cooler operation of the circuit, and the long–term reliable operation of the converter.

The major sources of heat within the converter are the power switch (NPN BJT), the resistive losses within the inductor, and losses associated with the output rectifier. These losses can be estimated by the following equations:

Power switch:

$$P_{D(sw)} \cong \frac{f_{sw} \times T_{on} \times I_{peak} \times V_{sat}}{2} \quad \textbf{Eqn. (11)}$$

Inductor:

$$P_{D(L0)} \cong 2I_{pk} \times 2R_{winding} \quad \textbf{Eqn. (12)}$$

Output rectifier:

$$P_{D(rect)} \cong I_{OUT(Vfwd)} \quad \textbf{Eqn. (13)}$$

The thermal resistance ($R_{th(j-a)}$) of the SA57255-XX is approximately 220 °C/W, assuming the device is soldered to a 2 oz. copper FR4 fiberglass circuit board, and that the minimum footprint was used (copper just under the leads). A rule of thumb in PCB design is that the thermal resistance can be reduced by 30% for each doubling of the copper area close to the device. This effect diminishes for areas greater than five times the minimum PCB footprint. If you take advantage of this rule, thermal resistance can be reduced by using wide copper lands when connecting to the leads of the major power-producing parts. These PCB traces should almost fill the areas surrounding the converter parts to conduct heat away from the device. For demanding applications, additional heat dissipation area can be created by placing a copper island on the opposite side of the PCB from each wide trace and connecting it to the trace with vias (plated thru holes).

The junction temperature can be estimated by Equation (14).

$$T_j \cong (P_D \times R_{th(j-a)}') + T_{amb(max)} \quad \textbf{Eqn. (14)}$$

Where:

P_D is the power dissipation (W).

$R_{th(j-a)}'$ is the effective thermal resistance with the additional copper (°C/W).

T_{amb} is the highest local expected ambient temperature (°C).

PACKING METHOD

The SA57255-XX is packed in reels, as shown in Figure 26.

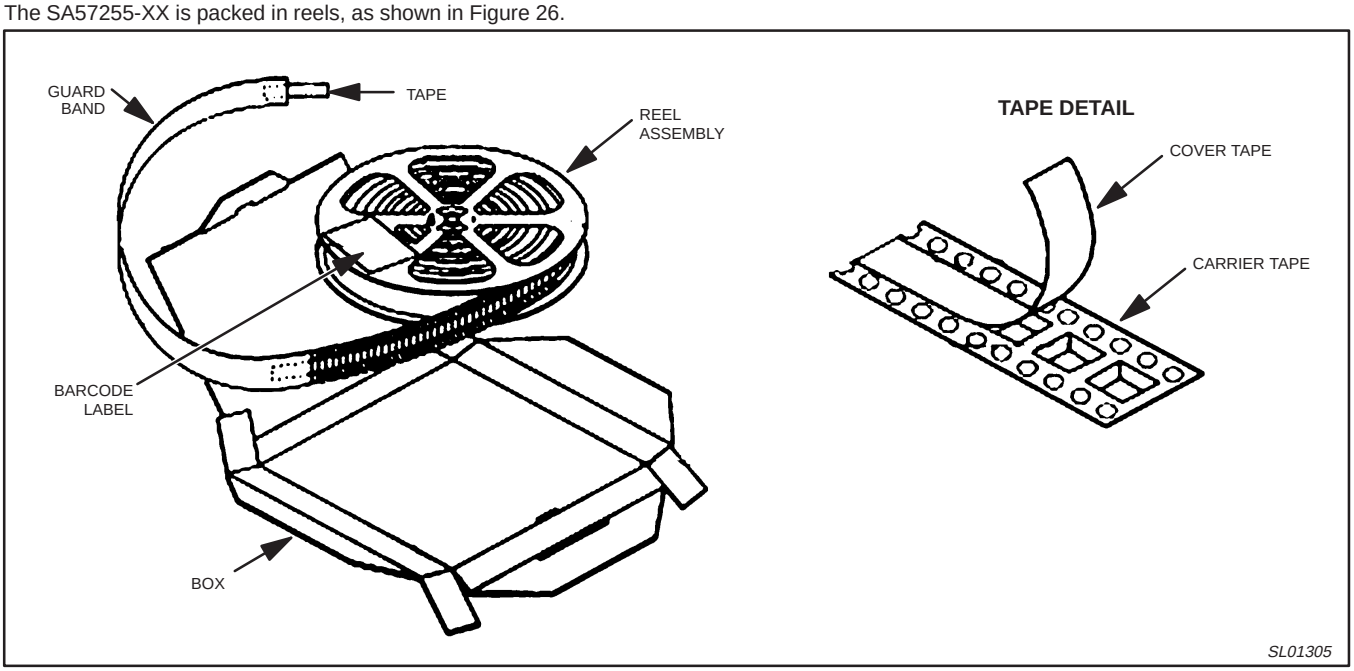
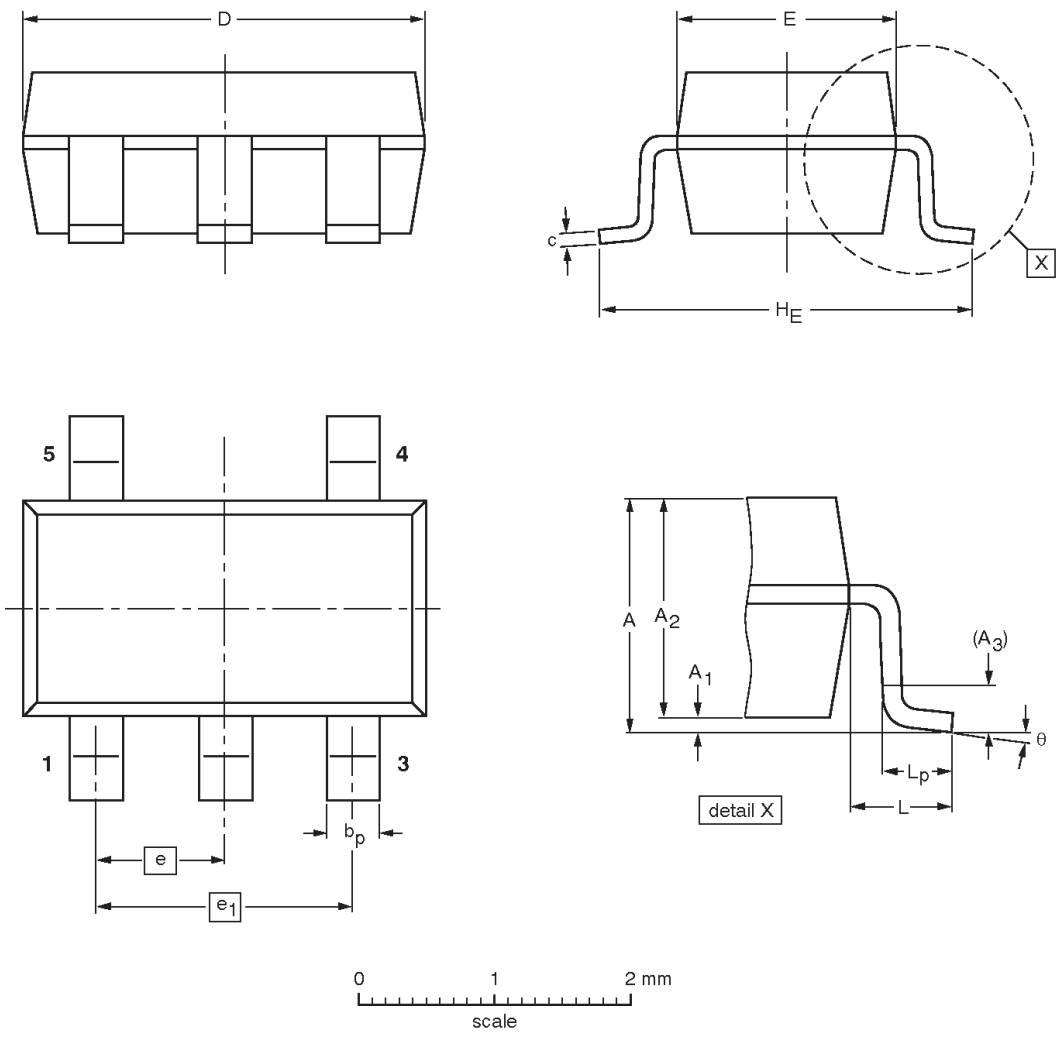


Figure 26. Tape and reel packing method.

Plastic small outline package; 5 leads; body width 1.6 mm **SOP003**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	e_1	H_E	L	L_p	θ
mm	1.35	0.15 0.05	1.2 1.0	0.25	0.50 0.25	0.22 0.08	3.0 2.7	1.7 1.5	0.95	1.9	3.0 2.6	0.6	0.55 0.35	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP003		MO-178				~~03-06-25~~ 03-10-07

CMOS switching regulator (PWM controlled) SA57255-XX

REVISION HISTORY

Rev	Date	Description
_2	20031111	**Product data (9397 750 12318). ECN 853-2273 30332 of 09 September 2003. Supersedes data of 2001 Aug 01 (9397 750 08904).** Modifications: ● Change package outline version to SOP003 in Ordering information table and Package outline sections.
_1	20010801	**Product data (9397 750 08904). ECN 853-2273 26807 of 01 August 2001.**

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Level	Data sheet status [1]	Product status [2] [3]	Definitions
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